Clean Version of Amended Specification Paragraphs

Title:STRUCTURE AND METHOD FOR IMPROVED SIGNAL PROCESSING
Applicant:Leonard Forbes
Serial No.: 10/057,225
Docket: 303.506US4

The paragraph beginning at page 1, line 5:

This application is a Continuation of U.S. Serial No. 09/560,777, filed April 28, 2000, now issued as U.S. Patent No.6,413,825 July 2, 2002, which is a Divisional of U.S. Serial No. 09/145,100, filed September 1, 1998, now issued as U.S. Patent No.6,104,068 August 15, 2000, which are incorporated herein by reference.

The paragraph beginning at page 8, line 1:

The RF circuit 100 may include a mixer circuit, a frequency multiplier, a heterodyne receiver, or any equivalent analog circuit structure. The RF circuit 100 includes a dual-gated metal-oxide semiconducting field effect transistor (MOSFET) 101, or transistor 101. In one embodiment, the dual-gated MOSFET is a vertical MOSFET such as, for example, the vertical MOSFET shown and described in co-pending Application Serial No. 08/889,462, entitled "Memory Cell Having A Vertical Transistor with Buried Source/Drain And Dual Gates," filed on July 8, 1997, now U.S. Patent No.6,150,687, which application is incorporated herein by reference. In an alternative embodiment, the dual-gated MOSFET is a lateral MOSFET such as, for example, the lateral MOSFET shown and described in co-pending Application Serial No. 09/050,281, entitled "Circuits and Methods for Dual-Gated Transistors," filed on March 30, 1998, now U.S. Patent No.6,097,065, which application is incorporated herein by reference. The dual-gated MOSFET 101 extends outwardly from a substrate and includes a first and a second source/drain region, 104A and 104B respectively. The dual-gated MOSFET includes a body region 102 which has opposing sidewall surfaces, 106 and 108 respectively. The body region 102 is formed with appropriate doping concentrations and with an appropriately narrow width between the opposing sidewall surfaces, 106 and 108, such that body region can be fully depleted during MOSFET operation. A first gate 110 is located on, and opposes, a first one 106 of the opposing sidewall surfaces, 106 and 108 respectively. A second gate 112 is located on, and

opposes, a second one 108 of the opposing sidewall surfaces, 106 and 108 respectively. The threshold voltage (V_t) of the first gate 110 is dependent on the potential applied to the second gate 112.